REMARKS

In the Office Action of May 21, 2007, claims 1-27 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,659,780 ("Wu"). Applicant submits that claim 1 is distinguishable from Wu for several reasons. The Examiner asserts that the shift registers rs11-rs1n, rs21-rs2n and register rb constitute first and second memory elements operable to store blocks of data to be processed in accordance with claim 1. Applicant disagrees and submits that Figure 1 of Wu instead shows only one memory element, referred to as multiport memory M. To emphasize this difference, claim 1 is amended herewith to refer to first and second "memory units" rather than first and second "memory elements." Therefore, the processor shown in Figure 1 of Wu does not receive blocks of data from first and second memory units in accordance with claim 1. Furthermore, the individual registers rs11-rs1n, rs21-rs2n and rb of Wu do not each store blocks of data per claim 1. Therefore, claim 1 is not anticipated by Wu.

Claim 1 is also amended herewith to specify that it is directed to a media processing filter engine. Claim 1 as amended also specifies that the first memory element stores blocks of *media* data, that the second memory element stores blocks of *media* data, and that the SIMD processor receives blocks of *media* data from the first and second memory units and performs filtering operations on the blocks of *media* data. Applicant submits that Wu does not teach these aspects of claim 1. Therefore, Applicant submits that claim 1, and claims 1-9 depending thereon, are not anticipated by Wu.

Claim 10 includes limitations that are similar to those included in claim 1. Applicant submits that claim 10 is not anticipated by Wu for the reasons set forth above with respect to claim 1. Furthermore, claim 10 includes recitations of first and second memory units as well as first and second shift registers. The Examiner asserts that the first and second memory units of claim 10 are anticipated by the shift registers rs11-rs1n, rs21-rs2n and register rb. The Examiner does not specify which elements of Figure 1 of Wu anticipate the first and second shift registers of claim 10. Applicant would assume that the Examiner deems the shift registers rs11-rs1n and rs21-rs2n to constitute the first and second shift registers. However, the Examiner alleges that those shift registers rs11-rs1n and rs21-rs2n constitute the first and second memory units of claim 10. The Examiner cannot use the same element of Wu to teach two different elements of

claim 10. This illustrates the error in the Examiner's allegation that the shift registers rs11-rs1n, rs21-rs2n and register rb constitute first and second memory units per claim 10 (and claim 1). As asserted previously, Wu only teaches one memory unit, i.e., multiport memory M. Furthermore, Wu does not teach that the shift registers rs11-rs1n and rs21-rs2n selectively shift their contents by a predetermined number of bits corresponding to the size of a data element per claim 10. Therefore, Applicant submits that claim 10, and claims 11-18 depending thereon, are not anticipated by Wu.

Claim 19 includes limitations that are similar to those included in claims 1 and 10. Applicant submits that claim 19 is not anticipated by Wu for the reasons set forth above with respect to claims 1 and 10. Furthermore, Wu does not teach that the shift registers rs11-rs1n and rs21-rs2n selectively shift their contents by a predetermined number of bits corresponding to a multiple of the size of a data element per claim 19. Therefore, Applicant submits that claim 19, and claims 20-27 depending thereon, are not anticipated by Wu.

In view of the foregoing, Applicant respectfully requests allowance of claims 1-27.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Respectfully submitted,

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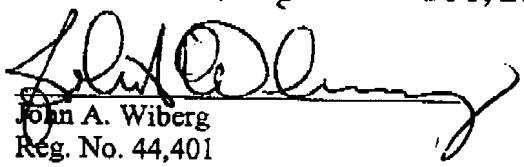
MCANDREWS, HELD & MALLOY, LTD.



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